ABSTRACT

The present invention is a means for constructing a high density memory device for very low cost by fabricating the device three dimensionally in layers. To keep points of failure low, address decoding circuits are included within each layer so that, in addition to power and data lines, only the address signal lines need be interconnected between the layers -- not the exponentially greater number of decoded rows and columns. Furthermore, to keep the testing of the device low in cost, a row and column interconnect means is disclosed for testing the any two-dimensional array within the three-dimensional array with a single continuity and short-circuit test.